

In the Claims

Cancel claims 1-60 without prejudice or disclaimer to the subject matter recited therein.

Add the following claims:

1 61. A method of making a semiconductor package device, comprising:
2 attaching a semiconductor chip to a metallic structure using an insulative adhesive,
3 wherein the chip includes a conductive pad, the metallic structure includes first and second
4 opposing surfaces and a conductive trace, the adhesive is disposed between the first surface and
5 the chip, the conductive trace includes a recessed portion, a non-recessed portion and opposing
6 outer edges between the first and second surfaces that extend across the recessed and non-
7 recessed portions, and the recessed portion is recessed relative to the non-recessed portion at the
8 second surface;

9 forming an encapsulant that contacts the chip, the first surface, the outer edges and the
10 recessed portion, wherein the encapsulant completely covers the chip, the outer edges and the
11 recessed portion without completely covering the non-recessed portion; and

12 forming a connection joint that electrically connects the conductive trace and the pad.

1 62. The method of claim 61, wherein the recessed portion is located between the non-
2 recessed portion and the chip.

1 63. The method of claim 61, wherein the outer edges are defined by first and second
2 slots in the metallic structure.

1 64. The method of claim 61, wherein the encapsulant contacts an entire side of the
2 chip opposite the pad.

1 65. The method of claim 61, wherein the encapsulant fills the recessed portion.

1 66. The method of claim 61, wherein the encapsulant is coplanar with the non-
2 recessed portion at the second surface.

1 67. The method of claim 61, wherein the encapsulant contacts substantially none of
2 the non-recessed portion at the second surface.

1 68. The method of claim 61, wherein the encapsulant is formed by transfer molding.

1 69. The method of claim 61, wherein the steps are performed in the sequence set
2 forth.

1 70. The method of claim 61, wherein the device is devoid of wire bonds, TAB leads
2 and solder joints.

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1 71. A method of making a semiconductor package device, comprising:
2 providing a metallic structure that includes first and second opposing surfaces, wherein
3 the metallic structure further includes a conductive trace and a pair of slots, the conductive trace
4 includes a recessed portion, a non-recessed portion and opposing outer edges defined by the slots
5 that are parallel to one another, extend between the first and second surfaces and extend across
6 the recessed and non-recessed portions, and the recessed portion is adjacent to the non-recessed
7 portion, coplanar with the non-recessed portion at the first surface and recessed relative to the
8 non-recessed portion at the second surface;
9 attaching the metallic structure to a semiconductor chip that includes a conductive pad,
10 wherein the first surface faces towards the chip and the second surface faces away from the chip;
11 forming an encapsulant that contacts the chip, the first surface, the outer edges and the
12 recessed portion, wherein the encapsulant fills the recessed portion and the slots without
13 completely covering the non-recessed portion; and
14 forming a connection joint that contacts and electrically connects the conductive trace and
15 the pad.

1 72. The method of claim 71, including forming the recessed portion and partially
2 forming the slots by selectively etching the metallic structure from the second surface towards
3 the first surface.

1 73. The method of claim 72, including partially forming the slots by selectively
2 etching the metallic structure from the first surface towards the second surface.

1 74. The method of claim 71, including removing the encapsulant from portions of the
2 slots adjacent to the non-recessed portion without removing the encapsulant from portions of the
3 slots adjacent to the recessed portion.

1 75. The method of claim 71, wherein the encapsulant contacts an entire side of the
2 chip opposite the pad.

1 76. The method of claim 71, wherein the encapsulant is coplanar with the non-
2 recessed portion at the second surface.

1 77. The method of claim 71, wherein the encapsulant contacts substantially none of
2 the non-recessed portion at the second surface.

1 78. The method of claim 71, wherein the encapsulant is formed by transfer molding.

1 79. The method of claim 71, wherein the steps are performed in the sequence set
2 forth.

1 80. The method of claim 71, wherein the device is devoid of wire bonds, TAB leads
2 and solder joints.

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1 81. A method of making a semiconductor package device, comprising:
2 providing a metallic structure that includes first and second opposing surfaces;
3 selectively etching the metallic structure to form a pair of slots that extend between the
4 first and second surfaces and a recessed portion that extends into the metallic structure at the
5 second surface towards the first surface and extends between the slots, wherein the metallic
6 structure further includes a non-recessed portion that extends between the slots, the recessed
7 portion is adjacent to the non-recessed portion, coplanar with the non-recessed portion at the first
8 surface and recessed relative to the non-recessed portion at the second surface, and the slots
9 define opposing edges that are parallel to one another, extend between the first and second
10 surfaces and extend across the recessed and non-recessed portions;

11 attaching the metallic structure to a semiconductor chip using an insulative adhesive,
12 wherein the chip includes a conductive pad, the first surface faces towards the chip, the second
13 surface faces away from the chip, and the recessed portion is located between the chip and the
14 non-recessed portion;

15 forming an encapsulant that contacts the chip, the first surface, the outer edges and the
16 recessed portion, wherein the encapsulant fills the recessed portion and the slots and the non-
17 recessed portion is exposed; and

18 forming a connection joint that contacts and electrically connects the metallic structure
19 and the pad.

20 82. The method of claim 81, including forming the recessed portion and partially
2 forming the slots by selectively etching the metallic structure from the second surface towards
3 the first surface.

1 83. The method of claim 82, including partially forming the slots by selectively
2 etching the metallic structure from the first surface towards the second surface.

1 84. The method of claim 81, including removing the encapsulant from portions of the
2 slots adjacent to the non-recessed portion without removing the encapsulant from portions of the
3 slots adjacent to the recessed portion.

1 91. A method of making a semiconductor package device, comprising:
2 providing a conductive trace that includes a terminal and a lead, wherein the terminal and
3 the lead are electrically connected to one another;
4 attaching the conductive trace to a semiconductor chip using an insulative adhesive,
5 wherein the chip includes a conductive pad;
6 forming a first insulative housing portion that contacts the chip and the lead without
7 contacting the terminal, wherein the lead protrudes laterally from and extends through the first
8 insulative housing portion;
9 forming a connection joint that contacts and electrically connects the conductive trace and
10 the pad; and
11 forming a second insulative housing portion that contacts the adhesive, the terminal and
12 the first insulative housing portion after forming the first insulative housing portion, wherein the
13 terminal protrudes downwardly from and extends through the second insulative housing portion,
14 and the first and second insulative housing portions form an insulative housing that surrounds the
15 chip.

1 92. The method of claim 91, wherein the terminal is within a periphery of the chip.

1 93. The method of claim 91, wherein the lead is outside a periphery of the chip.

1 94. The method of claim 91, wherein the first insulative housing portion contacts an
2 entire side of the chip opposite the pad.

1 95. The method of claim 91, wherein the first insulative housing portion is formed by
2 transfer molding, and the second insulative housing portion is formed without transfer molding.

1 96. The method of claim 91, wherein the insulative housing consists of the first and
2 second insulative housing portions.

1 97. The method of claim 91, wherein the insulative housing includes a top surface, a
2 bottom surface and peripheral side surfaces, the first insulative housing portion provides the top
3 surface, the side surfaces and a peripheral portion of the bottom surface, and the second
4 insulative housing portion provides a central portion of the bottom surface within the peripheral
5 portion of the bottom surface.

1 98. The method of claim 91, including:
2 bending the lead so that a distal end of the lead is moved vertically relative to the
3 terminal; and then
4 trimming the lead without trimming the terminal.

1 99. The method of claim 91, wherein the steps are performed in the sequence set
2 forth.

1 100. The method of claim 91, wherein the device is devoid of wire bonds, TAB leads
2 and solder joints.

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1 101. A method of making a semiconductor package device, comprising:
2 providing a conductive trace that includes a terminal and a lead, wherein the terminal and
3 the lead are electrically connected to one another;
4 attaching the conductive trace to a semiconductor chip using an insulative adhesive,
5 wherein the chip includes a conductive pad, the terminal is within a periphery of the chip, and the
6 lead is outside the periphery of the chip;
7 forming a first insulative housing portion that contacts the chip and the lead without
8 contacting the terminal;
9 forming a connection joint that contacts and electrically connects the conductive trace and
10 the pad; and
11 forming a second insulative housing portion that contacts the adhesive, the terminal and
12 the first insulative housing portion after forming the first insulative housing portion, wherein the
13 first and second insulative housing portions form an insulative housing that surrounds the chip,
14 the insulative housing includes a top surface, a bottom surface and four peripheral side surfaces,
15 the first insulative housing portion provides the top surface, the side surfaces and a peripheral
16 portion of the bottom surface, the second insulative housing portion provides a central portion of
17 the bottom surface within the peripheral portion of the bottom surface, the lead protrudes
18 laterally from and extends through the first insulative housing portion at one of the side surfaces,
19 and the terminal protrudes downwardly from and extends through the second insulative housing
20 portion at the central portion of the bottom surface.

1 102. The method of claim 101, wherein the first insulative housing portion contacts
2 and completely covers a side of the chip opposite the pad.

1 103. The method of claim 101, wherein the first insulative housing portion contacts
2 and completely covers four outer edges of the chip that are orthogonal to the pad.

1 104. The method of claim 101, wherein the first insulative housing portion is formed
2 by transfer molding, and the second insulative housing portion is formed without transfer
3 molding.

1 105. The method of claim 104, wherein the first insulative housing portion at the
2 peripheral portion protrudes below the second insulative housing portion at the central portion.

1 106. The method of claim 101, including bending the lead so that the lead includes first
2 and second corners, a first lateral portion between the insulative housing and the first corner, a
3 vertical portion between the first and second corners, and a second lateral portion between the
4 second corner and a distal end of the lead.

1 107. The method of claim 106, including trimming the lead thereby removing the first
2 and second corners, the vertical portion and the second lateral portion after bending the lead.

1 108. The method of claim 107, wherein trimming the lead excludes trimming the
2 terminal.

1 109. The method of claim 101, wherein the steps are performed in the sequence set
2 forth.

1 110. The method of claim 101, wherein the device is devoid of wire bonds, TAB leads
2 and solder joints.

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111. A method of making a semiconductor package device, comprising:

providing a metal base that includes first and second opposing surfaces;

etching the metal base to form a pair of slots that extend between the first and second surfaces, a first recessed portion that is recessed at the first surface and extends into the metal base towards the second surface and is spaced from the slots, and a second recessed portion that is recessed at the second surface and extends into the metal base towards the first surface and is between and adjacent to the slots, wherein the metal base includes a non-recessed portion that is spaced from the first recessed portion, adjacent to the second recessed portion and between and adjacent to the slots, the first recessed portion is recessed relative to the non-recessed portion at the first surface and coplanar with the non-recessed portion at the second surface, the second recessed portion is coplanar with the non-recessed portion at the first surface and recessed relative to the non-recessed portion at the second surface, and the second recessed portion and the non-recessed portion form a lead between the slots;

depositing a metal trace on the metal base, wherein the metal trace includes a terminal in the first recessed portion and a routing line on the first surface that contacts the lead;

attaching the metal base to a semiconductor chip using an insulative adhesive, wherein the chip includes a conductive pad, the first surface faces towards the chip, the second surface faces away from the chip, the terminal is between the pad and the second recessed portion, and the second recessed portion is between the terminal and the non-recessed portion;

forming a first insulative housing portion that contacts the chip and fills the slots and the second recessed portion without contacting the terminal;

removing the first insulative housing portion from a region of the slots adjacent to the non-recessed portion, wherein the lead protrudes laterally from and extends through the first insulative housing portion;

etching the metal base, thereby exposing the terminal and the adhesive;

forming a connection joint that contacts and electrically connects the routing line and the pad; and

forming a second insulative housing portion that contacts the terminal and the adhesive, wherein the terminal protrudes downwardly from and extends through the second insulative housing portion, and the first and second insulative housing portions form an insulative housing that surrounds the chip.

112. The method of claim 111, wherein etching the metal base to form the slots and the recessed portions includes:

forming a first etch mask on the first surface that includes openings that selectively expose the first surface;

forming a second etch mask on the second surface that includes openings that selectively expose the second surface;

applying a wet chemical etch through the openings in the first etch mask to selectively etch the first surface, thereby forming the first recessed portion and partially forming the slots;

applying a wet chemical etch through the openings in the second etch mask to selectively etch the second surface, thereby forming the second recessed portion and partially forming the slots;

removing the first etch mask; and

removing the second etch mask.

113. The method of claim 112, including:

simultaneously forming the first and second etch masks;

simultaneously applying the wet chemical etches to the first and second surfaces; and

simultaneously removing the first and second etch masks.

114. The method of claim 111, wherein depositing the metal trace includes:

forming a plating mask on the first surface that includes an opening that selectively exposes the first surface; and

electroplating the metal trace in the opening and on the exposed portion of the first surface.

115. The method of claim 111, wherein etching the metal base to expose the terminal and the adhesive includes:

depositing a protective coating on a portion of the lead that protrudes laterally from the first insulative housing portion; and then

5 applying a wet chemical etch that is selective of the metal base with respect to the
6 protective coating.

1 116. The method of claim 115, wherein depositing the protective coating includes:
2 forming a plating mask on a portion of the second surface within a periphery of the first
3 insulative housing portion that selectively exposes the portion of the lead that protrudes laterally
4 from the first insulative housing portion; and
5 electroplating the protective coating on the portion of the lead that protrudes laterally
6 from the first insulative housing portion.

1 117. The method of claim 111, wherein forming the second insulative housing portion
2 includes:
3 depositing an insulative layer that covers the terminal; and
4 selectively removing a portion of the insulative layer that covers the terminal, thereby
5 exposing the terminal without exposing a portion of the routing line that contacts the lead.

1 118. The method of claim 111, wherein forming the second insulative housing portion
2 includes:
3 depositing an insulative layer that conformally covers the terminal; and
4 globally removing a surface portion of the insulative layer, thereby exposing the terminal
5 without exposing a portion of the routing line that contacts the lead.

1 119. The method of claim 111, wherein the steps are performed in the sequence set
2 forth.

1 120. The method of claim 111, wherein the device is devoid of wire bonds, TAB leads
2 and solder joints.

1 121. A method of making a semiconductor package device, comprising the following
2 steps in the sequence set forth:

3 providing an insulative housing, a semiconductor chip, a terminal and a lead, wherein the
4 insulative housing includes a top surface, a bottom surface, and a peripheral side surface between
5 the top and bottom surfaces, the chip includes a conductive pad, the terminal protrudes
6 downwardly from and extends through the bottom surface, the lead protrudes laterally from and
7 extends through the side surface, the terminal and the lead are spaced and separated from one
8 another outside the insulative housing, and the terminal is electrically connected to the lead and
9 the pad inside the insulative housing and outside the chip;

10 singulating the lead from a lead frame; and

11 trimming the lead without trimming the terminal.

1 122. The method of claim 121, wherein trimming the lead includes trimming the
2 insulative housing.

1 123. The method of claim 122, wherein trimming the lead includes cutting the
2 insulative housing and a conductive trace that includes the lead using a laser.

1 124. The method of claim 122, wherein trimming the lead includes removing a
2 rectangular peripheral portion of the insulative housing that includes a rectangular peripheral
3 portion of the top surface, a rectangular peripheral portion of the bottom surface and the side
4 surface.

1 125. The method of claim 121, wherein trimming the lead includes removing a portion
2 of the lead that protrudes from the insulative housing, thereby leaving the terminal as the only
3 electrical conductor that protrudes from the insulative housing and is electrically connected to the
4 pad.

1 126. The method of claim 121, wherein trimming the lead includes removing a portion
2 of the lead that extends vertically beyond the insulative housing.

1 127. The method of claim 121, wherein trimming the lead includes removing a portion
2 of the lead that includes two bent corners.

1 128. The method of claim 121, wherein trimming the lead includes removing the lead.

1 129. The method of claim 128, wherein removing the lead includes cutting a routing
2 line that extends between the terminal and the lead, is integral with the terminal and is plated on
3 the lead.

1 130. The method of claim 129, wherein cutting the routing line includes cutting
2 through the insulative housing between the top and bottom surfaces.

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1 131. A method of making a semiconductor package device, comprising the following
2 steps in the sequence set forth:

3 providing an insulative housing, a semiconductor chip, a plurality of terminals and a
4 plurality of leads, wherein the insulative housing includes a top surface, a bottom surface, and
5 peripheral side surfaces between the top and bottom surfaces, the bottom surface includes a
6 peripheral portion adjacent to the side surfaces and a central portion within the peripheral portion
7 and spaced from the side surfaces, the peripheral portion protrudes downwardly from the central
8 portion, the chip includes a plurality of conductive pads, the terminals are arranged in an array
9 that protrudes downwardly from and extends through the central portion of the bottom surface,
10 the leads are arranged in opposing rows that protrude laterally from and extend through the side
11 surfaces, the terminals and the leads are spaced and separated from one another outside the
12 insulative housing, and each of the terminals are electrically connected to one of the leads and
13 one of the pads inside the insulative housing and outside the chip;

14 singulating the leads from a lead frame; and

15 trimming the insulative housing and the leads without trimming the terminals.

1 132. The method of claim 131, wherein trimming the insulative housing and the leads
2 includes simultaneously trimming the insulative housing and the leads.

3 133. The method of claim 131, wherein trimming the insulative housing and the leads
4 includes cutting the insulative housing and conductive traces that include the leads using a laser.

1 134. The method of claim 131, wherein trimming the insulative housing and the leads
2 includes removing portions of the leads that protrude from the insulative housing, thereby
3 leaving the terminals as the only electrical conductors that protrude from the insulative housing
4 and are electrically connected to the pads.

1 135. The method of claim 131, wherein trimming the insulative housing and the leads
2 includes removing portions of the leads that extend vertically beyond the insulative housing.

1 136. The method of claim 131, wherein trimming the insulative housing and the leads
2 includes removing portions of the leads that include two bent corners.

1 137. The method of claim 131, wherein trimming the insulative housing and the leads
2 includes removing the leads and creating peripheral side surfaces of the insulative housing and
3 distal ends of routing lines that are coplanar with one another, and the routing lines are integral
4 with the terminals.

1 138. The method of claim 131, wherein trimming the insulative housing and the leads
2 includes removing all portions of the device outside a periphery of the central portion of the
3 bottom surface.

1 139. The method of claim 131, wherein trimming the insulative housing and the leads
2 converts the device from a TSOP package to a grid array package.

1 140. The method of claim 131, wherein trimming the insulative housing and the leads
2 converts the device to a chip scale package.

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